# Arm Cortex-R52+

Product Brief

## Benefits

### 1. Real-Time Performance

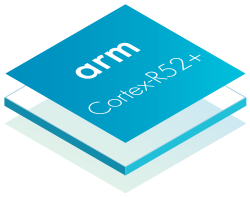
High-performance multicore clusters of Cortex-R52+ CPUs deliver real-time responsiveness for deterministic systems with low latency requirements. Software compatible to Cortex-R52.

### 2. Software Separation

Hardware-enforced software separation enables Freedom From Interference (FFI) for safety-related tasks, reducing code certification, saving time, cost, and effort. It supports multiple operating systems for simplified application consolidation.

### 3. Simplified Integration

Reduces integration effort for chip makers and software developers by removing the need for additional integration IP and enabling flexible allocation of resources.




## Overview

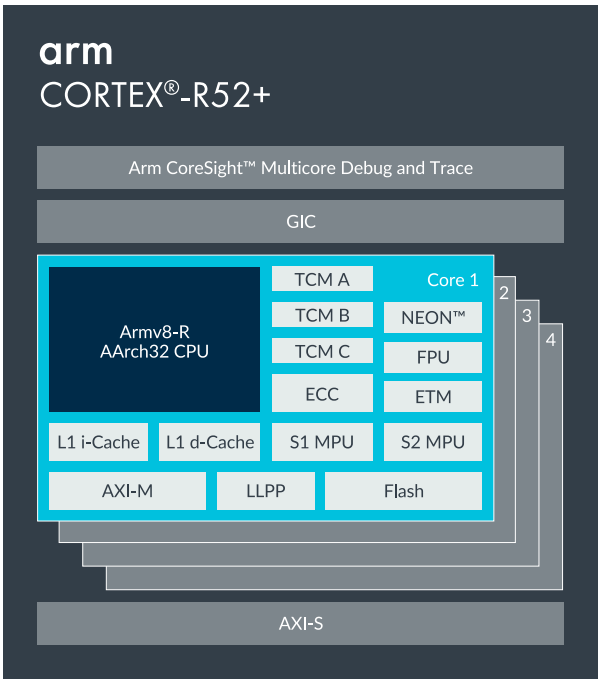
The Cortex-R52+ continues the legacy of advanced real-time processors with deterministic high performance and advanced functional safety. It implements the 32-bit Armv8-R architecture and offers improved configurability and enhanced granularity for virtualization, helping systems to extend separation of virtual machines.

Cortex-R52+ addresses a range of applications, such as high-performance domain controllers for vehicle powertrain and chassis systems or as a safety island providing protection in complex ADAS and autonomous drive systems.

## Safety Ready

Arm Cortex-R52+ is part of Arm's Safety Ready portfolio, a collection of Arm IP that has been through various and rigorous levels of functional safety systematic flows and development.

Learn more at www.arm.com/safety



## Specifications

| Architecture | Armv8-R |
|---|---|
| Instruction Set | Arm and Thumb-2. Supports DSP instructions and a configurable floating-point unit either with single precision or double precision and Neon. |
| Microarchitecture | 8-stage pipeline with instruction pre-fetch, branch prediction, superscalar in order execution. Binary compatible with the Cortex-R52. |
| Up to quad-core | Multi-processor configurations of up to four integer CPUs or up to four lockstep CPU pairs within a single cluster. |
| Dual Core Lock Step (DCLS) | Redundant Cortex-R52+ cores in lockstep for fault detection in dependable systems with optional split/lock configuration to decouple checking core enabling independent execution. |
| Safety Package | Licensable, extended safety package to simplify product safety implementation. |
| Self Test Technology | High fault coverage through integrated 'built-in self test' capabilities (BIST). Optional integrated programmable memory BIST controller. |
| Software Test Libraries | Licensable library of software tests which can be called and flexibly executed during run time, offering non-destructive fault coverage of the processor's logic. |
| Cache controllers | Optional Harvard memory architecture with write-through instruction and data caches. Cache sizes are independently configurable for 4K to 32K. |
| Tightly-Coupled Memories | Optional tightly coupled memory available for deterministic or low-latency applications such as interrupt service routines or frequently used data. Up to three flexibly configurable TCMs memories, each up to 1Mbyte. |
| Generic Interrupt Controller | Fully integrated generic interrupt controller (GIC). Configurable to support from 32 to 960 interrupts with priority-based interrupt handling. |
| Memory Protection Unit (MPU) | Two stage MPUs interdependently configurable to support 24 regions from 64 bytes upward, enabling real-time virtualization. |
| Floating-Point Unit (FPU) | Single or double precision floating point unit with up to 32x 64-bit or 16x 128-bit double precision registers. |
| Advanced SIMD (NEON) | Optional advanced SIMD supporting integer or single precision results. Implemented together with double precision floating point. |
| ECC | Single-bit error correction and double-bit error detection for cache and TCM memories with hard error protection. |
| Port Protection | Configurable port protection enabling ECC on Level 2 interfaces for data and address, or data only. |
| Primary Port | 128-bit AMBA AXI-4 bus manager port for Level-2 memory and peripheral access, with optional protection. |
| TCM Access Port | 128-bit full AMBA AXI-4 bus low-latency subordinate port for low-latency access to the TCMs for high speed streaming of data in and out of the processor, with optional protection. |
| Low Latency Peripheral Port (LLPP) | A dedicated 32-bit AMBA AXI port supporting 128Mbytes addressable range to integrate latency-sensitive peripherals more tightly with the processor, with optional protection. |
| Flash Interface Port | Per core dedicated 128-bit AMBA AXI port to integrate latency-sensitive memory tightly to a specific core within the processor cluster. Optional configurable ECC protection. |
| Configurable boot | Optional low speculation mode out of reset. |
| Bus Interconnect Protection | Optional additional protection to guard against errors in the interconnect switch fabric, and end-to-end transaction protection. |

## Related Products

### Safety Documentation Package

Arm's Safety Documentation Package for Cortex-R52+ provides information for partners implementing safety-related features. It includes comprehensive details on specific product safety features, verification and Failure Mode Effects & Diagnostic Analysis (FMEDA). The Safety Documentation package simplifies integration of the Cortex-R52+ into systems with ISO 26262 and IEC 61508 requirements.

### Software Test Libraries

Arm Software Test Libraries provide diagnostic coverage to address functional safety requirements for ISO 26262 and IEC 61509 systems with flexible execution scheduling, minimizing the run-time impact on the application.

### Fast Models

Fast Models are accurate, flexible programmer's view models of Arm IP, allowing the development of software, such as drivers, firmware, operating systems and applications, which can be widely deployed independently to silicon availability.

### Cycle Models

Cycle Models are cycle accurate, flexible models of Arm IP, allowing you to precisely model software performance, such as drivers and firmware prior to silicon availability.

### Arm Development Studio

A professional package equipping engineering teams to bring products to market faster and cost effectively. Combining the best of Arm and Keil development tools and middleware, Development Studio seamlessly covers the entire product lifecycle, from SoC architecture exploration to software integration and testing. A safety-certified version of the tool is also available and includes qualification kit and documentation.

### CoreSight Debug and Trace

Arm offers a portfolio of IP to support debug features to observe or modify the state of parts of the design, while trace features allow continuous collection of system information. System developers can select the most appropriate CoreSight components based on their system requirements.