Certificate / Certificat

Zertifikat / 合格証

Arm 1711153 C007

exida hereby confirms that the:

Arm Cortex-M33 Processor (Revisions: r1p0 and r0p4)

Arm Ltd. Cambridge, Great Britain

Has been assessed per the relevant requirements of:

ISO 26262:2011 Parts 2, 4, 5, 7, 8, 9 and 10

IEC 61508:2010 Parts 1 and 2

and meets requirements providing a level of safety integrity to:

Systematic Capability: ASIL D / SC 3 (SIL 3 Capable)

Safety related function:
It is assumed that a system-level technical safety concept allocates technical safety requirements to the Cortex-M33 processor – which was developed as a Safety Element out of Context (SEooC) or a compliant item – around the following functions:

- Execution of instructions, generating the correct result and executing in the right order
- Correct response to stimuli like interrupts and events
- Correct usage of buses according to defined protocols
- Correct usage of coprocessors with a defined interface

Application restrictions:
The Cortex-M33 processor shall be used according to the requirements described in the Arm Cortex-M33 Processor Safety Manual.

Evaluating Assessor

Certifying Assessor

The manufacturer may use the marks:

Revision 1.1 Jan 23, 2021
Surveillance Audit Due
May 1, 2023

ISO/IEC 17065
PRODUCT CERTIFICATION BODY
#1004

Arm Cortex-M33 Processor (Rev. r1p0, r0p4)

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Arm Cortex-M33 Processor (Revisions: r1p0 and r0p4)

Systematic Capability: ASIL D / SC 3 (SIL 3 Capable)

Arm Cortex-M33 Processor and Safety Integrity Mechanisms

The Arm® Cortex®-M33 processor is a general-purpose microprocessor design IP implementing the ARMv8-M architecture with the Main Extension. It consists of fixed and optional components. The Cortex-M33 processor implements several fault detection and control functionalities, primarily to support preventing and controlling systematic faults on a system-on-chip (SoC) or software level:

- Memory Protection Unit (MPU)
- Security Attribution Unit (SAU)
- Implementation Defined Attribution Unit
- Exceptions
- Bus-Fault Exception

The Cortex-M33 processor shall be configured and integrated into an SoC and used as described in the safety manual. The safety manual also describes several assumptions-of-use about safety mechanisms that shall be implemented by the integrator or user of the processor core.

Systematic Capability: ASIL D / SC 3 (SIL 3 Capable)

The Arm Cortex-M33 processor is a hardware Safety Elements out of Context (SEooC) per ISO 26262-10. The development, as documented by Arm, meets the applicable ASIL D design specification, implementation and verification requirements of ISO 26262, parts 4-9, as guided by ISO 26262-10, and the functional safety management requirements per ISO 26262-2. It also meets the applicable requirements for SIL 3 capability (SC 3) from IEC 61508, parts 1-2.

No Random Capability

The Arm Cortex-M33 processor does not include any safety mechanisms for the prevention and mitigation of random hardware faults. Instead, Arm expects that the integrator and user of the Cortex-M33 processor specifies, implements and validates appropriate safety concepts and safety mechanisms against random hardware faults on SoC or system level.

Consequently, the capability of the Arm Cortex-M33 processor to cope with random hardware faults is excluded from the scope of this certification. It must be addressed in an assessment or certification of the element integrating the Cortex-M33 processor.

The following documents are a mandatory part of this certification:

Assessment Report:	Arm 17/11-153 R007, V1 R1
Safety Manual:	Arm® Cortex®-M33 Processor Safety Manual (Rev. r1p0)
	Arm® Cortex®-M33 Processor Safety Manual (Rev. r0p4)

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